The AlInAs–GaInAs HEMT for Microwave and Millimeter-Wave Applications

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(Invited Paper)

Abstract—This paper reviews the status of lattice-matched and pseudomorphic AlInAs–GaInAs HEMT's grown on InP substrates. The best lattice-matched devices with 0.1 μm gate length had a transconductance $g_m = 1080$ mS/mm and unity current gain cutoff frequency $f_T = 178$ GHz, whereas similar pseudomorphic HEMT's had $g_m = 1160$ mS/mm and $f_T = 210$ GHz. Single-stage *V*-band amplifiers demonstrated 1.3 and 1.5 dB noise figures and 9.5 and 8.0 dB associated gains for the lattice-matched and pseudomorphic HEMT's, respectively. The best performance achieved was $F_{min} = 0.8$ dB with $G_a = 8.7$ dB.

I. Introduction

FUTURE DoD and NASA communication and radar systems will require high-performance millimeter-wave (MMW) devices that operate in the 30–100 GHz range. Some of the most important applications are low-noise amplifiers for receiver front ends and power amplifiers for phased array radars. New materials systems and device structures are needed to meet the stringent performance requirements of these advanced systems. Noise figures must be reduced in existing frequency bands and the operating frequency must be extended to *W*-band and above. Phased array radar systems require affordable high-efficiency monolithic microwave and MMW integrated circuit (MIMIC) components. High-speed digital circuits (e.g., prescalers) will require FET's with gain–bandwidth products f_T greater than 200 GHz. Components based on FET's made with GaAs and related ternaries are very well suited for these applications. By optimizing the materials system, layer design, and device dimensions, researchers have reported devices with f_T's above 200 GHz, extrinsic transconductances greater than 1000 mS/mm [1], and *K*-band [2] and *V*-band [3] noise figures less than 0.5 dB and 1.0 dB, respectively. A three-stage *V*-band LNA constructed by GE exhibited a minimum noise figure of 3.0 dB with an associated gain of 22.0 dB over the frequency band of 60 to 65 GHz [2]. In addition, digital IC's with gate delays less than 5 ps and static frequency dividers operating up to 26.7 GHz have been demonstrated [4]. This paper presents a comparison of the leading materials systems for FET's, reasons for the enhanced performance of the $Al_{0.48}In_{0.52}As$–$Ga_{0.47}In_{0.53}As$ material system, and state-of-the-art performance of devices and circuits fabricated in this material system.

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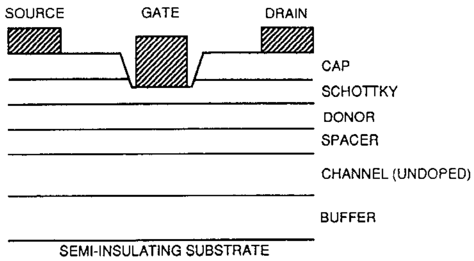
II. Device Structure

Microwave and millimeter-wave FET's based on both GaAs and InP have emerged over the last decade in response to requirements for three-terminal devices with higher frequency, lower noise, and higher power. The key characteristics which describe the unique features of the different device structures are shown in Fig. 1. The spiked-doped GaAs FET structure shown is optimized for low-noise applications. With 0.1 μm gate length, the state-of-the-art f_T of this device is ≥ 100 GHz with an extrinsic transconductance of 500 to 700 mS/mm [5]. The emergence of the AlGaAs–GaAs HEMT with the separation of the electron donor layer from the conducting channel improves the device performance to $f_T \sim 120$ GHz and $g_m \sim 600$ to 750 mS/mm [6]. Adding a small percentage of indium to the GaAs channel in the AlGaAs–InGaAs HEMT decreases the band gap of the channel, and electron mobility and conduction band discontinuity are correspondingly increased. Channel conductivity is increased because both the well charge and the channel mobility are increased. The resulting f_T and g_m are 150 GHz and 700 to 900 mS/mm, respectively [7]. The addition of 10 to 20 percent indium caused a significant lattice mismatch with the GaAs substrate, resulting in a strain in the as-grown crystal, hence the descriptor "pseudomorphic" InGaAs HEMT.

Recently, the $Al_{0.48}In_{0.52}As$–$Ga_{0.47}In_{0.53}As$ HEMT grown lattice matched on InP substrates has provided even further device performance improvements. With 0.1 μm gate lengths, these lattice-matched GaInAs HEMT's have



DEVICE TYPE

LAYER	GaAs MESFET	AlGaAs HEMT	AlGaAs-InGaAs PSEUDOMORPHIC HEMT	AlInAs-GaInAs HEMT	AlInAs-GaInAs PSEUDOMORPHIC HEMT
CAP	n^+GaAs	n^+GaAs	n^+GaAs	n^+GaInAs	n^+GaInAs
SCHOTTKY	n GaAs	n AlGaAs	n AlGaAs	n^- AlInAs	n^- AlInAs
DONOR LAYER		n^+AlGaAs	n^+AlGaAs	n^+AlInAs	n^+AlInAs
CHANNEL	n^+GaAs	p^- GaAs	p^- $In_{0.15}Ga_{0.85}As$	n^- $Ga_{0.53}In_{0.47}As$	n^- $Ga_{0.32}In_{0.68}As$
BUFFER LAYER	p^- GaAs	p^- GaAs	p^- GaAs	n^- AlInAs	n^- AlInAs
S I SUBSTRATE	GaAs	GaAs	GaAs	InP	InP

Fig. 1. Schematic FET device structures for GaAs FET, AlGaAs–GaAs–InGaAs pseudomorphic HEMT, AlInAs–GaInAs HEMT, and AlInAs–GaInAs pseudomorphic HEMT.

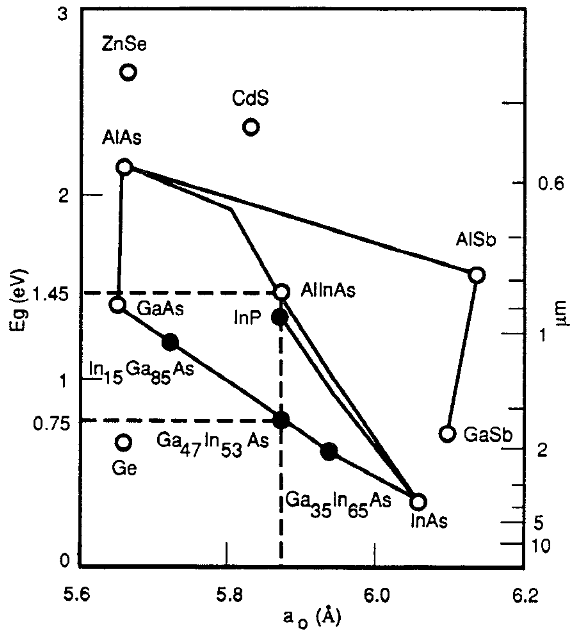


Fig. 2. Plot of energy band gap versus lattice constant.

f_T ~170 GHz and g_m ~1000 mS/mm [3]. By increasing the indium concentration to 62 percent, we have demonstrated $f_T = 210$ GHz and $g_m = 1160$ mS/mm [1].

The relative performance of each of these FET's depends on many factors, the most important of which are electron drift mobility, peak velocity, and channel charge density. The plot of band gap versus lattice constant shown in Fig. 2 provides some insight into the impact of choosing a particular materials system. The GaAs FET has almost all of the dopant donor sites in the spike region. Hence, the mobility in the conducting channel (spike layer) is relatively low. The total channel charge is limited only by tunneling and breakdown voltage considerations. The lattice-matched $Al_xGa_{1-x}As$–GaAs HEMT structure, though promising for MMW low-noise and cryogenic digital applications, suffers from a small conduction band discontinuity ($\Delta E_c = 0.2$ eV for $x = 0.25$), which in turn results in lowered sheet charge density ($n_s \sim 1\times10^{12}$ cm^{-2}) and relatively poor charge confinement. Furthermore, the DX center concentration in the $Al_xGa_{1-x}As$, which increases with aluminum mole fraction, causes undesirable threshold voltage shifts and drain current collapse at cryogenic temperatures.

The pseudomorphic $Al_xGa_{1-x}As$–$In_yGa_{1-y}As$ HEMT grown on GaAs substrate offers solutions to some of these problems by increasing the conduction band discontinuity with a smaller band gap $In_yGa_{1-y}As$ channel. Furthermore, the $In_yGa_{1-y}As$ channel offers superior transport properties because of enhanced carrier confinement in the channel and slightly higher mobility. This has resulted in impressive MMW noise and power performance from these devices.

A superior alternative to the GaAs-based HEMT systems is the $Al_{0.48}In_{0.52}As$–$Ga_{0.47}In_{0.53}As$ modulation doped structure grown lattice matched on InP. The large conduction band discontinuity ($\Delta E_c \sim 0.51$ eV) coupled with the high doping efficiency of silicon in the AlInAs ($N_D > 1\times10^{19}$ cm^{-3}) establishes a large two-dimensional electron density ($n_s > 4\times10^{12}$ cm^{-2}) in the GaInAs channel. In addition, the excellent electron mobility ($\mu > 10000$ cm^2/V·s) and high peak velocity ($v_p \sim 2.7\times10^7$ cm/s) in $Ga_{0.47}In_{0.53}As$ result in very low parasitic resistances, high transconductance, and excellent high-frequency performance.

The advantages gained by introducing a pseudomorphic $Ga_{0.47-u}In_{0.53+u}As$ channel are similar to those in the GaAs system, namely, increased conduction band discontinuity, sheet charge density, and carrier confinement coupled with a higher electron mobility. Workers at the University of Michigan have investigated both single- and double-heterojunction HEMT's. They obtained an intrinsic f_T of 38 GHz from 1.4-μm-long-gate, single-heterojunction HEMT's [8]. Devices with 1-μm-long gates fabricated on double-heterojunction pseudomorphic HEMT's showed an extrinsic f_T of 37 GHz and an f_{max} of 66 GHz [9].

III. Device Fabrication

Based on the theoretical advantages of the InP-based devices, we began an experimental program to determine whether these advantages could be realized in practice. All of our modulation doped structures were grown on (100) iron-doped InP substrates in a Riber 2300 system equipped with a 3 in. rotating substrate holder. The substrate temperature was held constant during growth at approximately 500°C. Growth rates varied from 0.75 to 1.0 μm/h. A typical device structure is shown in Fig. 3.

First, a 250-nm-thick AlInAs buffer was grown, followed by a 40-nm-thick AlInAs–GaInAs superlattice. The

GaInAs	n^+ CONTACT LAYER (5 nm)
AlInAs	UNDOPED BARRIER LAYER (20 nm)
AlInAs	n^+ DONOR LAYER (12.5 nm)
AlInAs	UNDOPED SPACER LAYER (2 nm)
GaInAs	UNDOPED CHANNEL (40 nm)
AlInAs/GaInAs	UNDOPED SUPERLATTICE
AlInAs	UNDOPED BUFFER LAYER
InP	SEMI-INSULATING SUBSTRATE

Fig. 3. AlInAs–GaInAs HEMT structure for *V*-band low-noise applications.

AlInAs layer served the dual purpose of separating the active layer from the InP surface and providing a high band gap layer which confines the electrons in the active GaInAs channel, thus reducing the FET output conductance. The superlattice also serves two other important purposes. It smooths the AlInAs growth front, minimizing interface roughness scattering, resulting in higher electron mobility in the channel [10]. Also, the superlattice can getter out-diffusing impurities from the substrate, which further improves the transport properties of the active channel. Next, a 40-nm-thick GaInAs channel was grown, followed by a 2 nm undoped AlInAs spacer. The AlInAs donor layer was then grown, 12.5 nm thick, and doped with silicon at $4\times10^{18}/cm^3$. This was followed by a 20-nm-thick undoped AlInAs layer that serves as a Schottky-barrier-enhancing layer, and the structure was capped by a 5-nm-thick n^+ GaInAs contact layer [11].

The major differences in the epitaxial layer design between the lattice-matched wafer (L) and the pseudomorphic wafer (P) were

i) the indium mole fraction: 53 percent in the lattice-matched case and 62 percent in the pseudomorphic wafer;
ii) the thickness of the GaInAs channel: 40 nm in wafer L and 27 nm in wafer P.

The reduced thickness in wafer P ensured that the critical thickness for the formation of misfit dislocations due to lattice mismatch was not exceeded. The properties of the two-dimensional electron gas (2DEG) are a strong function of the nature and magnitude of the silicon doping in the AlInAs, the width and composition of the $Ga_{0.47-u}In_{0.53+u}As$ conductive channel, and the spacer layer thickness. As the doping in the AlInAs donor layer is increased, the number of electrons available for transfer into the GaInAs to form the 2DEG is increased. The available electrons are shared between the AlInAs–GaInAs heterojunction at the channel–donor layer interface and the donor–contact layer interface. The relative distribution is determined by (i) the distance of the doped region from the two interfaces and (ii) the nature of the doping (i.e., uniform or planar). The width of the channel affects the 2DEG mobility through the interface roughness scattering at the inverted AlInAs–GaInAs interface. Lastly, as has been stated before, increasing the indium mole fraction in

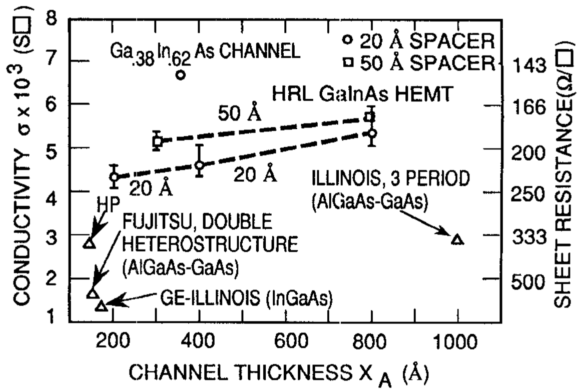


Fig. 4. AlInAs–GaInAs HEMT channel conductivity as a function of channel and spacer thickness at room temperature. HP data are for a $Al_{0.25}Ga_{0.75}As–In_{0.25}Ga_{0.75}As$ pseudomorphic structure.

the channel increases both the electron affinity of the channel (and hence n_s) and the electron mobility. The most important and easily measurable parameter which characterizes the channel is the conductivity of the 2DEG, which governs the parasitic resistances in the device. Fig. 4 summarizes the effects of the various parameters on the conductivity (or resistivity) of the 2DEG and illustrates the superiority of the AlInAs–GaInAs system over the AlGaAS–GaAs and AlGaAs–InGaAs systems. Further details of the growth condition have been presented previously [12].

The process sequence for device fabrication has been described elsewhere [13] and is listed below:

a) device isolation by mesa etching or ion implantation;
b) ohmic contact metal evaporation and lift-off;
c) ohmic metal alloy;
d) optical gate formation by lift-off;
e) T-gate formation by E-beam lithography and subsequent lift-off;
f) overlay metallization.

To determine the impact of the superior materials properties on device performance, we fabricated HEMT's with 1.0, 0.2, and 0.1 μm gate lengths. The extrinsic transconductance of the 1.0 μm gate length device is 600 mS/mm. This impressive performance at such a long gate length is primarily due to the low parasitic resistances in the structure resulting from the high 2DEG density and mobility. The extrinsic transconductances of 50- and 200-μm-wide latticed-matched devices with 0.2 and 0.1 μm gate lengths are 800 and 1080 mS/mm, respectively. Both devices have been characterized from 45 MHz to 26.5 GHz on a Cascade Microtech® probe station. The current gain h_{21} of the devices was calculated using the measured S parameters and the unity current gain cutoff frequency f_T, determined by extrapolating at 6 dB/octave. The data are presented in Fig. 5. The 50-μm-wide devices with gate lengths of 0.2 and 0.1 μm exhibited an f_T equal to 120 and 140 GHz, respectively. The 200-μm-wide device with 0.1 μm gate length exhibited an $f_T = 170$ GHz.

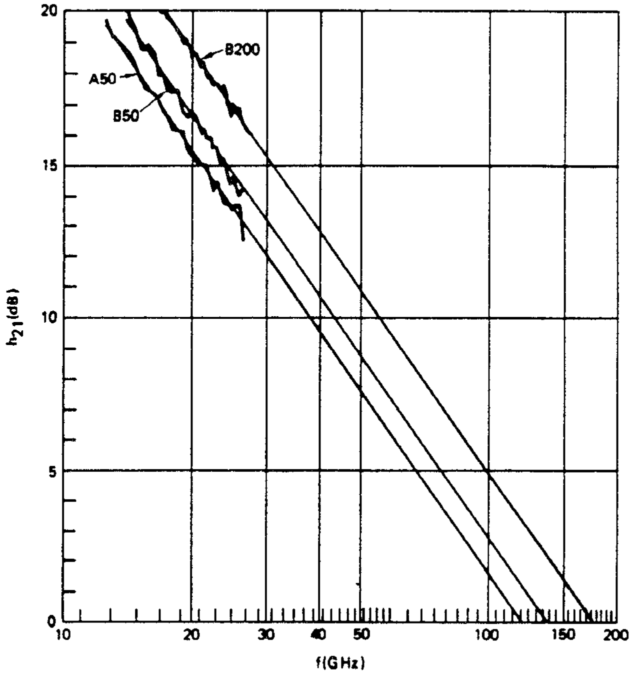


Fig. 5. Current gain versus frequency of 0.2 and 0.1 μm gate length HEMT's for 50- and 200-μm-wide devices.

The dc $I-V$ characteristics of AlInAs–GaInAs HEMT's exhibit anomalous drain current behavior [14] (a kink) at a V_{ds} ranging from 300 to 500 mV. This kink has been attributed to weak avalanching, carrier injection into or through the high-band-gap barrier or buffer, and trap-related phenomena in the AlInAs buffer layer. This kink can potentially degrade the noise margin and power dissipation of digital circuits. Workers at Cornell University and at Allied Signal [15] have related the kink in MESFET's and AlInAs–GaInAs–AlInAs HEMT's to traps in the structure by studying the frequency-dependent output conductances of the device. They have established that the kink is absent in the RF $I-V$ characteristics.

We have fabricated 1.0-μm-gate HEMT's grown by MBE with an AlInAs buffer and GaInAs buffer, to determine if buffer design is related to the occurrence of the kink. AlInAs is known to have a high trap density, while GaInAs has a low trap density. Previous attempts to fabricate GaInAs–AlInAs HEMT's with GaInAs buffers failed because of poor pinch-off of the channel. To overcome this problem, we grew a thick superlattice (AlInAs–GaInAs) at the substrate–buffer interface and at the buffer layer–active channel interface. The sheet charge and mobility (300 K) of the two structures, as inferred from Hall measurements, were $n_s = 4\times10^{12}/\text{cm}^2$ with $\mu_s = 8800$ cm^2/V·s for the AlInAs buffer and $n_s = 3.95\times10^{12}/\text{cm}^2$ with $\mu_s = 10\,000$ cm^2/V·s for the GaInAs buffer. Observations of dc transconductances of 550 to 650 mS/mm were made for both 1.0-μm-gate-length devices. The device with the AlInAs buffer exhibited the usual kink at $V_{DS} \approx 0.400$ mV. However, the device fabricated with the GaInAs buffer showed no kink. Excellent pinch-off and comparable output conductances were observed for both structures.

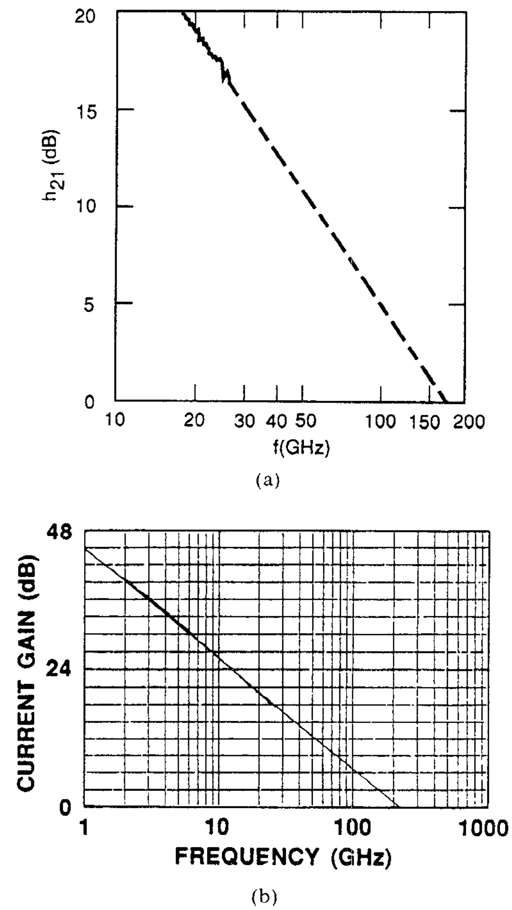


Fig. 6. Plot of the current gain (h_{21}) versus frequency of (a) the lattice-matched HEMT and (b) the pseudomorphic HEMT.

The magnitude of the kink in the AlInAs buffer devices has also been found to be greatly affected by the application of a side gate voltage. These effects all point to trap depopulation at high electric fields in the AlInAs buffer as the origin of the kink effect [14].

IV. Device Performance

The transconductance of a lattice-matched HEMT with a 0.1-μm-long gate was ~1060 mS/mm, whereas that of a similar pseudormorphoric HEMT was 1160 mS/mm. The S parameters of 200-μm-wide devices were measured on-wafer. The resulting h_{21} data are presented in Fig. 6(a) and (b). A typical lattice-matched $Al_{0.48}In_{0.52}As–Ga_{0.47}In_{0.53}As$ HEMT exhibited $f_T = 175$ GHz, whereas a similarly fabricated pseudomorphic $Al_{0.48}In_{0.52}As–Ga_{0.38}In_{0.62}As$ HEMT exhibited a record value of 210 GHz. This is the first report of a transistor with a unity current gain cutoff frequency greater than 200 GHz. The $f_{\max}$ of the transistor was ~ 300 GHz, obtained from S parameter measurements.

The minimum noise figure performance of a microwave transistor can be approximated by Fukui's equation [16]:

$$F_{\min} = 1 + K_f \cdot \frac{f}{f_T}\sqrt{g_m(R_g + R_s)}\,.$$

Bulk GaInAs has long been recognized as an excellent

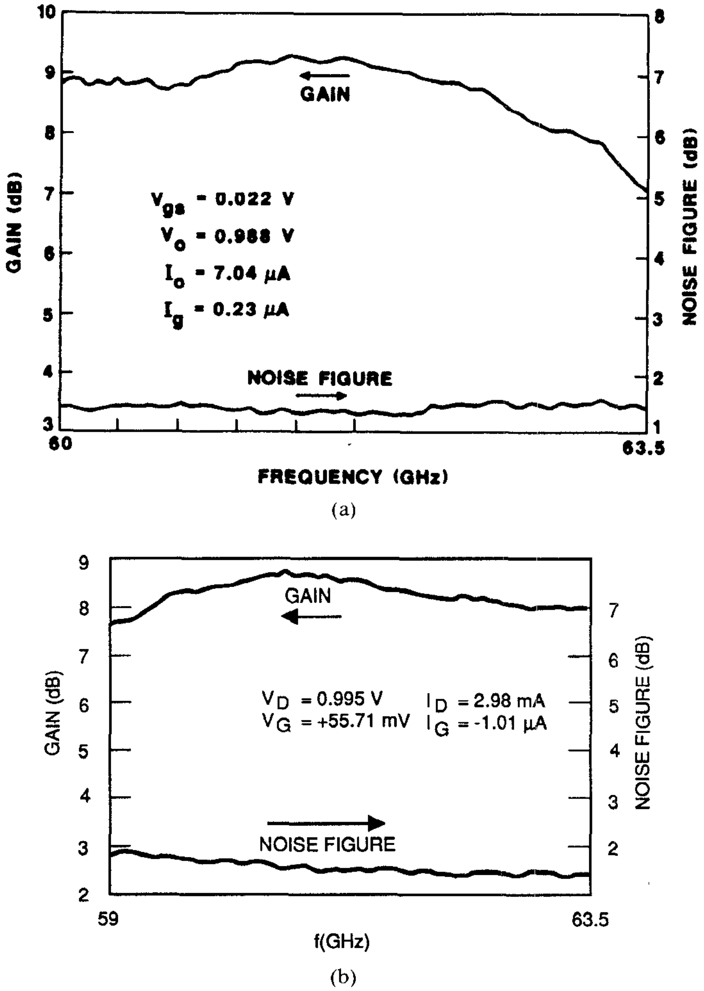


Fig. 7. Minimum noise figure and associated gain of single-stage amplifiers constructed with (a) lattice-matched HEMT's and (b) pseudomorphic HEMT's.

material for low-noise transistors due to:

i) the high electron mobility, which reduces the parasitic source resistance in the transistor, which in turn lowers thermal noise;
ii) the large Γ–L valley separation (0.55 eV) compared to GaAs (0.31 eV), which reduces the intervalley scattering (low K_f);
iii) the high peak velocity v_p in $Ga_{0.47}In_{0.53}As$ ($v_p \sim 2.7 \times 10^7$ cm/s) versus GaAs ($v_p \sim 2.0 \times 10^7$ cm/s), which leads to a higher f_T in submicrometer-gate-length devices.

The AlInAs–GaInAs HEMT exhibits all of these advantages to a greater degree because of i) higher electron mobility in the undoped channel and ii) higher f_T than bulk GaInAs FET's.

The gain and the noise figure of 50-µm-wide devices were measured between 60 and 63.5 GHz. The data are presented in Fig. 7(a) (lattice matched HEMT) and (b) (pseudomorphic HEMT). The data represent the waveguide-to-waveguide performance of single-stage amplifiers with no corrections for circuit losses. The minimum noise figure of the lattice-matched HEMT amplifier was 1.3 dB and the associated gain was 9.4 dB. The minimum noise figure of the pseudomorphic HEMT amplifier was 1.5 dB and the associated gain was 8 dB. Our best result to date has been for a lattice-matched HEMT with 0.2 µm gate length, which exhibited a $F_{min} = 0.8$ dB and a $G_a = 8.7$ dB at 63.5 GHz (Fig. 8). Since the amplifier noise and gain performance is a very strong function of circuit tuning, the difference in amplifier performance is not substantial enough to draw conclusions about differences in device noise performance.

V. Conclusions

AlInAs–GaInAs modulation doped structures grown by MBE on InP have demonstrated excellent electronic properties. Extremely high sheet charge densities ($n_s \sim 4 \times 10^{12}/cm^2$) and room-temperature mobilities ($\mu \sim 9500$ $cm^2/V \cdot s$) have been achieved. HEMT 's with 0.1 µm gate lengths have exhibited an $f_T \simeq 170$ GHz, whereas pseudomorphic $Al_{0.48}In_{0.52}As$–$Ga_{0.38}In_{0.62}As$ HEMT's with 0.1 µm gates have demonstrated extrinsic $f_T \simeq 210$ GHz. Single-stage amplifiers using 0.2-µm-gate HEMT's have demonstrated a minimum noise figure of 0.8 dB and an associated gain of 8.7 dB. These results confirm the tremendous impact that AlInAs–GaInAs HEMT's will have on millimeter-wave electronics.

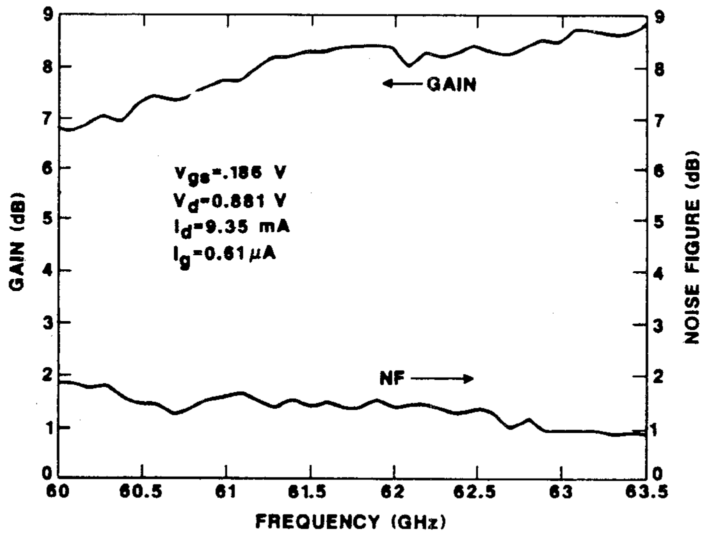


Fig. 8. *V*-band noise figure and associated gain data for a single-stage amplifier.

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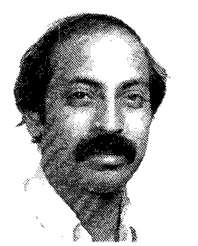

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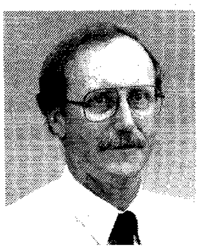

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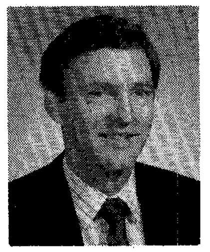
Paul T. Greiling (S'64–M'69–SM'82–F'85) received the B.S.E.E. and B.S. Math degrees in 1963, the M.S.E.E. degree in 1964, and the Ph.D. degree in 1970 from the Unviersity of Michigan. Ann Arbor.

He joined the faculty of Electrical Engineering at Northeastern University, Boston, MA, in 1970. While at Northeastern he consulted for Lincoln Laboratory, M.I.T., in the area of IMPATT diodes. In 1972 he joined the faculty of Electrical Sciences and Engineering at the University of California, Los Angeles, where he did research on the theoretical analysis and experimental characterization of microwave solid-state devices. He consulted for local industry on millimeter-wave semiconductor devices. In 1976, he was a Visiting Faculty Member at Sandia Laboratories, Albuquerque, NM, working on GaAs FET's. In 1976 he joined the staff at Hughes Research Laboratories, Malibu, CA, where he has been responsible for the design, modeling, and testing of GaAs digital IC's.

Dr. Greiling was selected as a Distinguished Microwave Lecturer by the Microwave Theory and Techniques Society for 1984–85 and presented a lecture entitled "High-Speed Digital IC Performance Outlook" to MTT chapters throughout the U.S., Europe, and Japan. At present he is Manager of the GaAs Devices and Circuits Department at Hughes Research Laboratories, working on high-speed GaAs logic circuits and is an Adjunct Professor in the Electrical Sciences and Engineering Department at UCLA. Dr. Greiling is a member of the MTT-S AdCom, Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.



Charles F. Krumm (S'63–M'70–SM'87–F'89) was born in Macomb, IL, on August 3, 1941. He received the Assoc. in Science degree from Grand Rapids Junior College in 1961, and the B.S.E., M.S.E., and Ph.D. degrees, all in electrical engineering, from the University of Michigan in 1961, 1963, and 1970 respectively.

From 1969 to 1976 he was with the Raytheon Company Research Division in Massachusetts. There he worked on high-power Gunn devices, surface acoustic wave devices, and Si bipolar transistors and liquid and vapor phase epitaxial growth of GaAs. He was the leader of the initial GaAs FET fabrication team at Raytheon and also led the first transfer of that technology into production at Raytheon. In 1976 he joined the Hughes Research Laboratories in Malibu, CA, where he held a series of increasingly responsible positions, most recently as manager of the Microelectronics Laboratory. His role at Hughes included responsibility for the development of advanced Si and GaAs device and integrated circuit technologies. The activities in his laboratory covered a wide range of topics, covering ion implantation, 0.1 μm electron beam lithography, molecular beam and metal organic epitaxy, and ultra-high-speed circuit design, simulation, layout, and testing of digital integrated circuits up to 30 GHz and devices up to 100 GHz. In March 1989 he transferred to the Hughes Radar Systems Group, where he is assistant manager of the Hughes MIMIC program. He has filed numerous patent disclosures and has two U.S. patents awarded. He is the author of two book chapters and over 50 conference publications and presentations. He is also a graduate of the Raytheon and Hughes management programs and the UCLA Executive Management Program.

Dr. Krumm has served on the technical program committees of several conferences, including the Device Research Conference and the International Electron Devices Meeting. He has served as technical program chairman and general chairman of the IEEE Cornell Conference. He has also been an invited panelist at the International Solid State Circuits Conference and the International Microwave Theory and Techniques Symposium. He has served on several government committees addressing semiconductor competitiveness issues. Dr. Krumm is a member of Phi Kappa Phi, Sigma Xi, and Eta Kappa Nu.